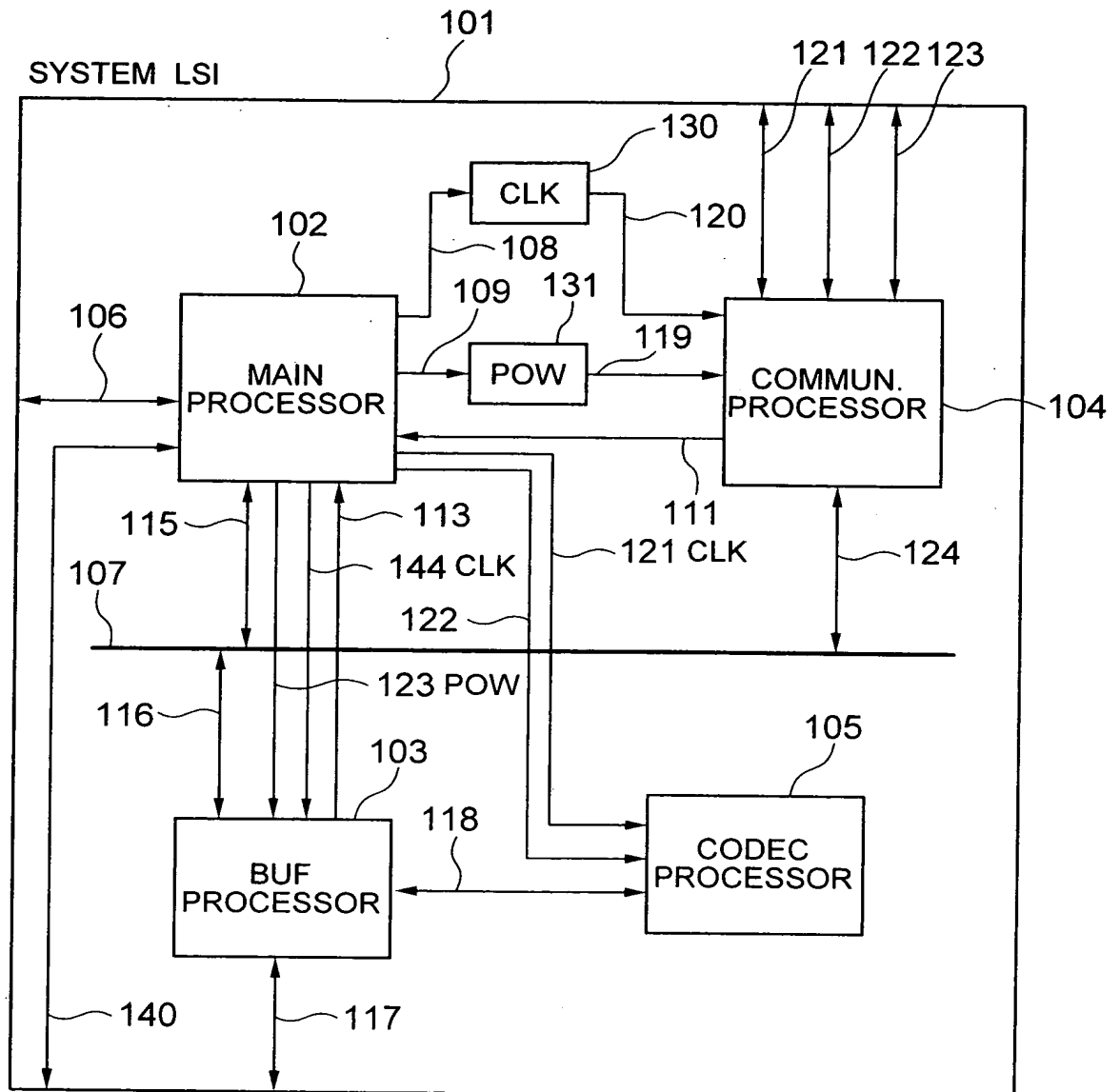


FIG. 1



102

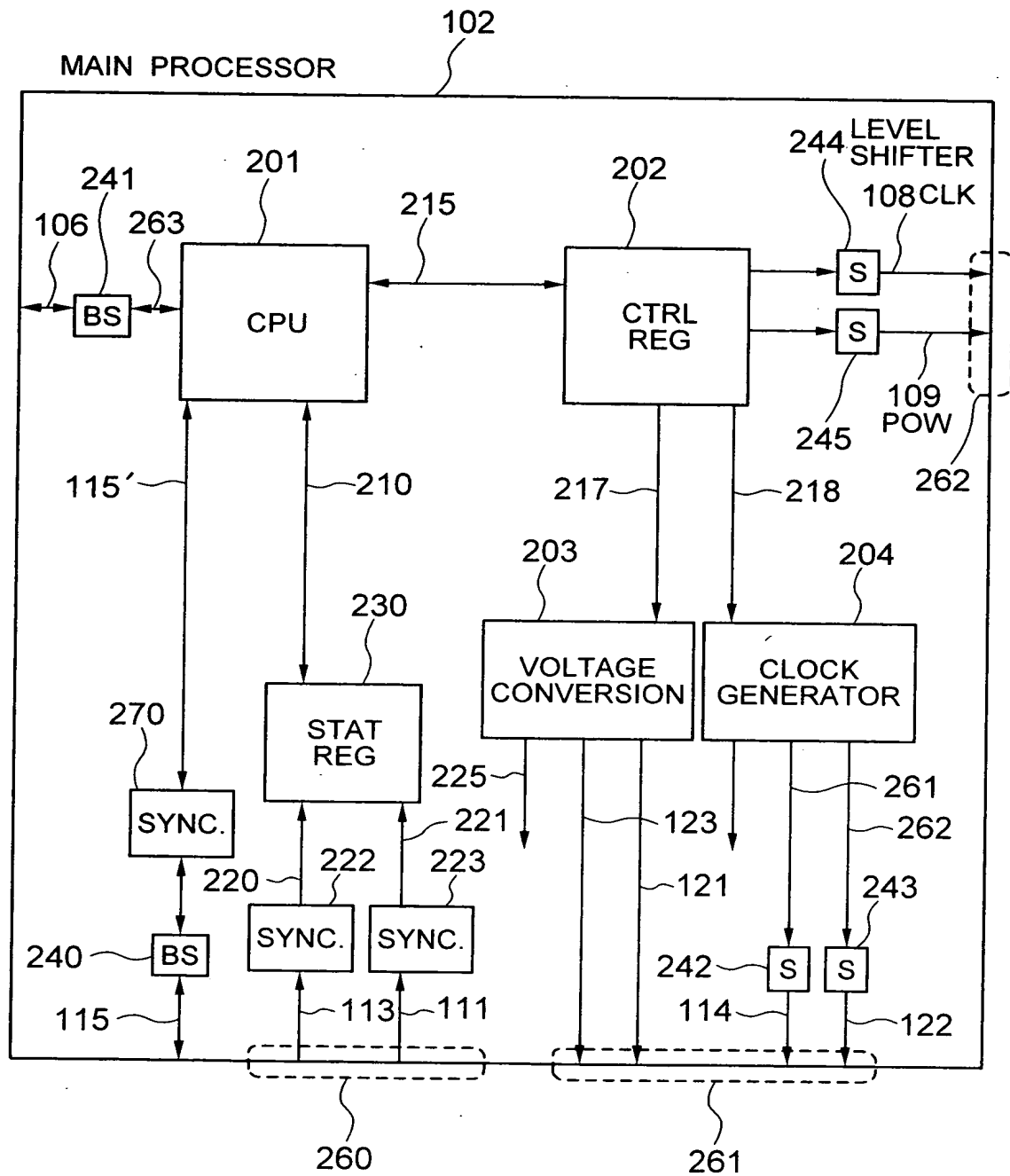


FIG. 3

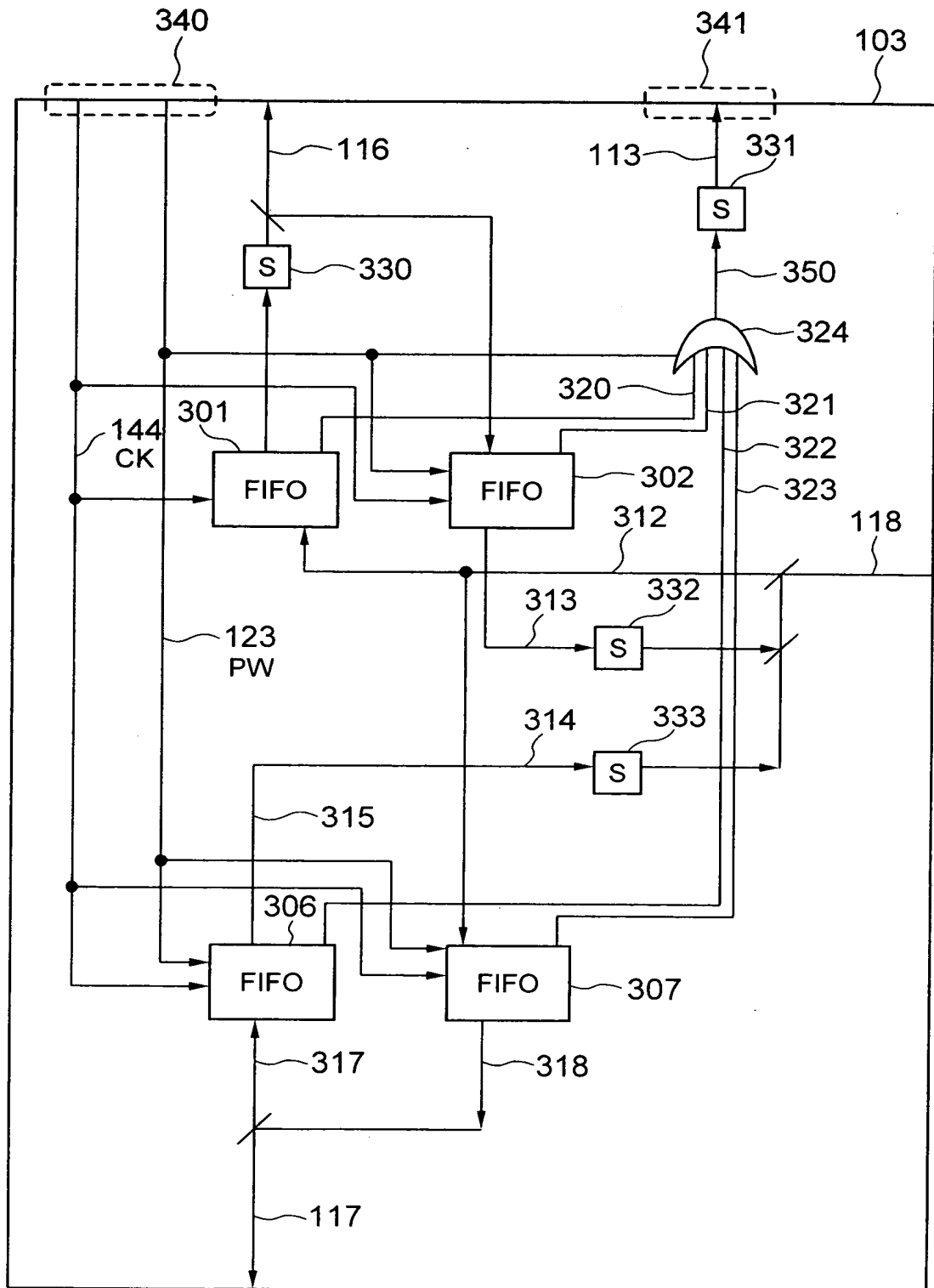


FIG. 4A

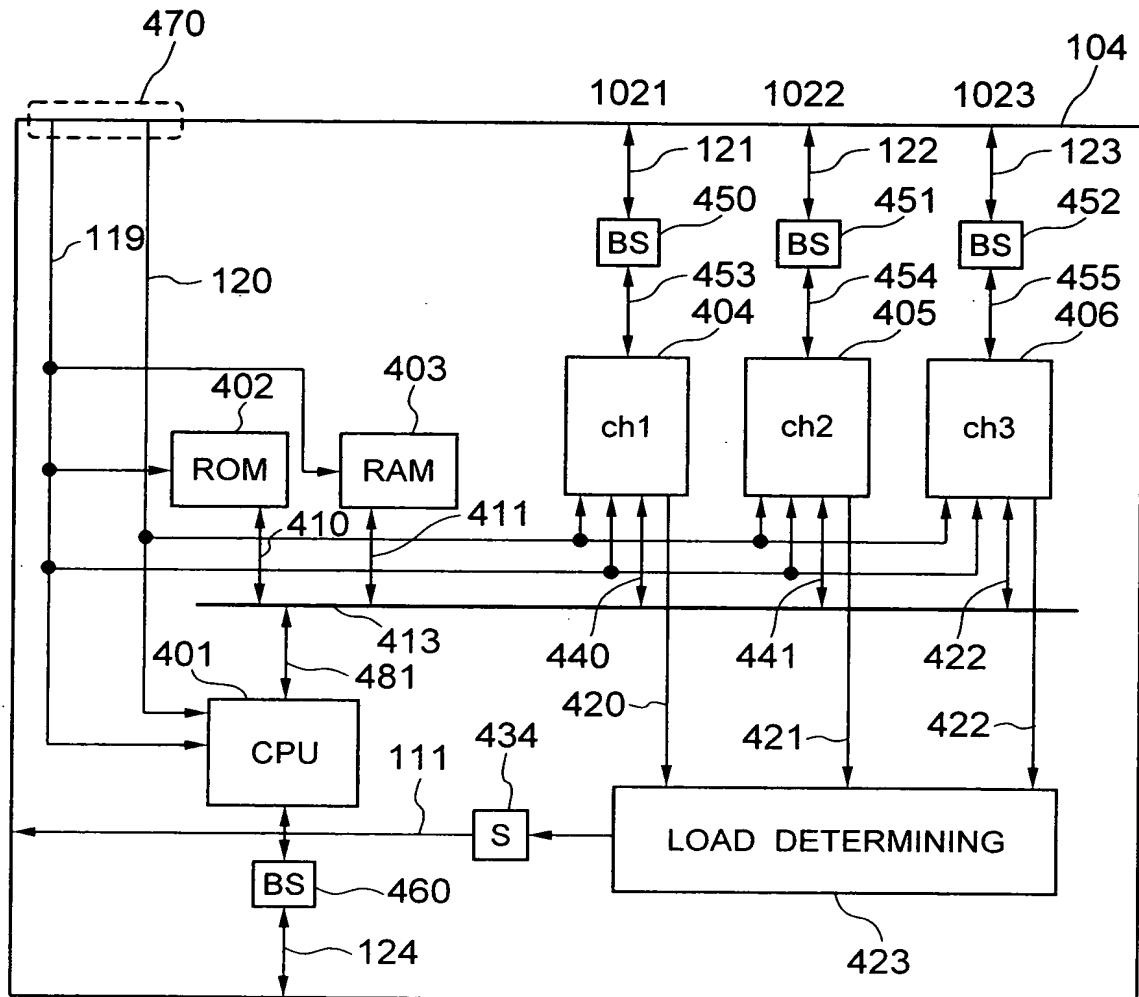


FIG. 4B

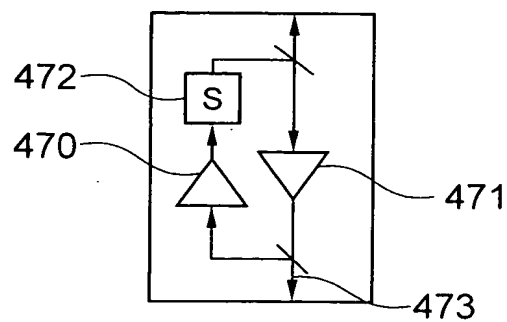


FIG. 5

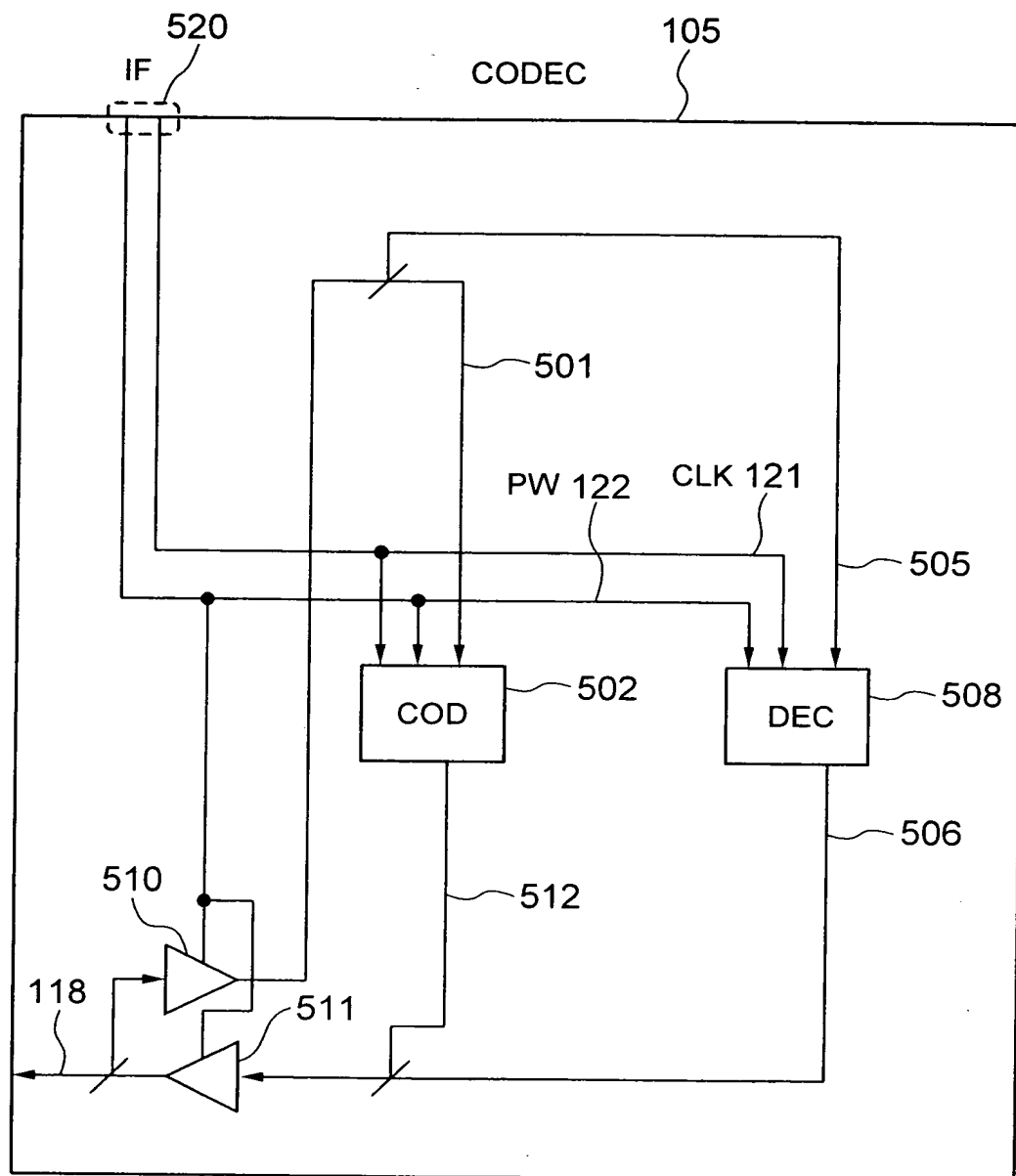


FIG. 6

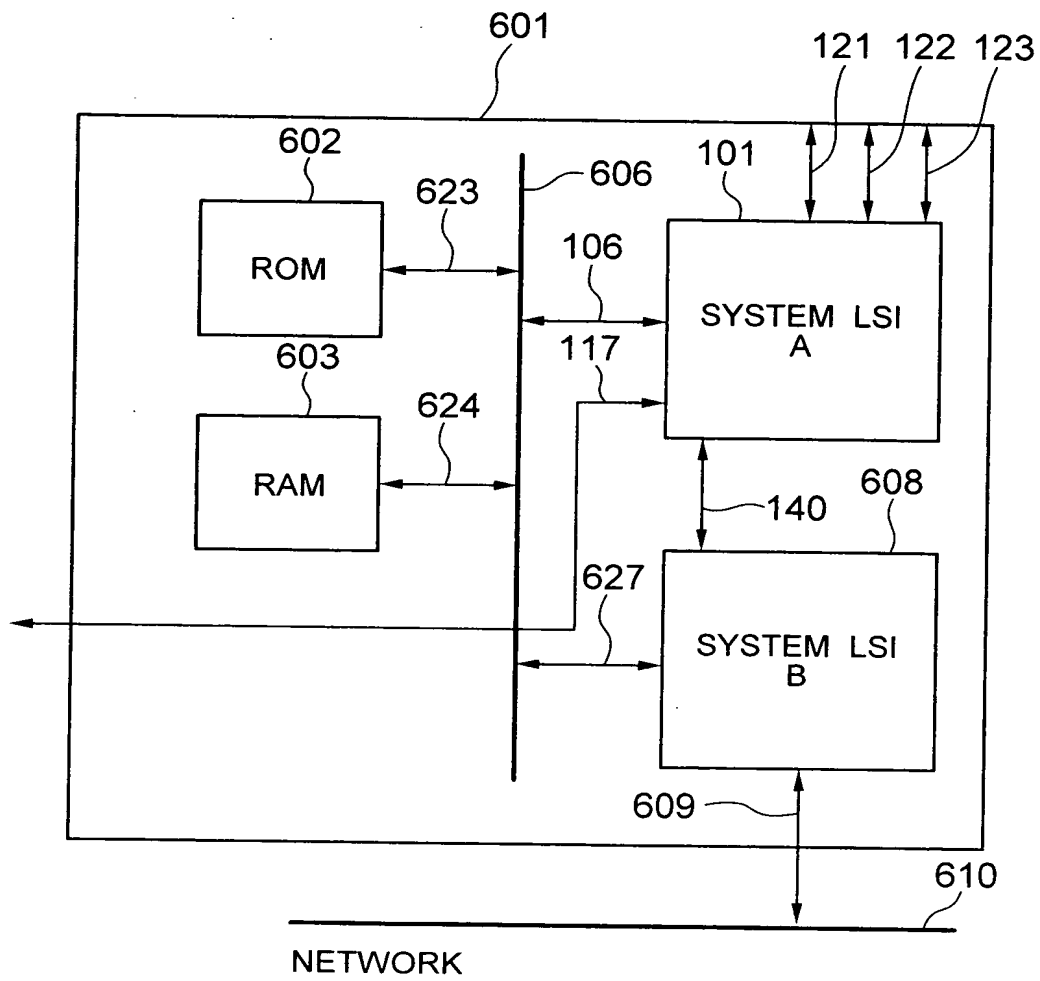


FIG. 7

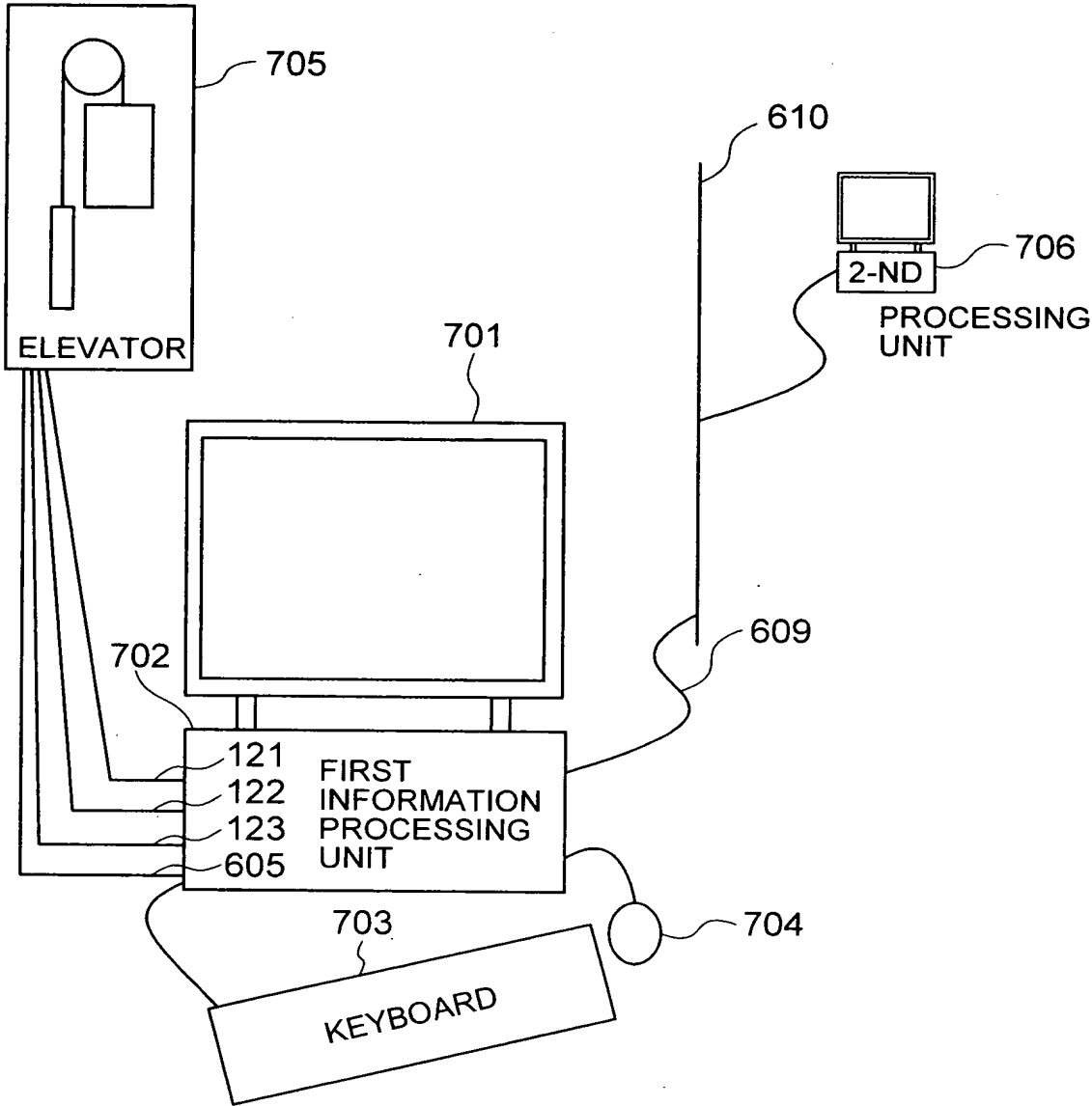


FIG. 8

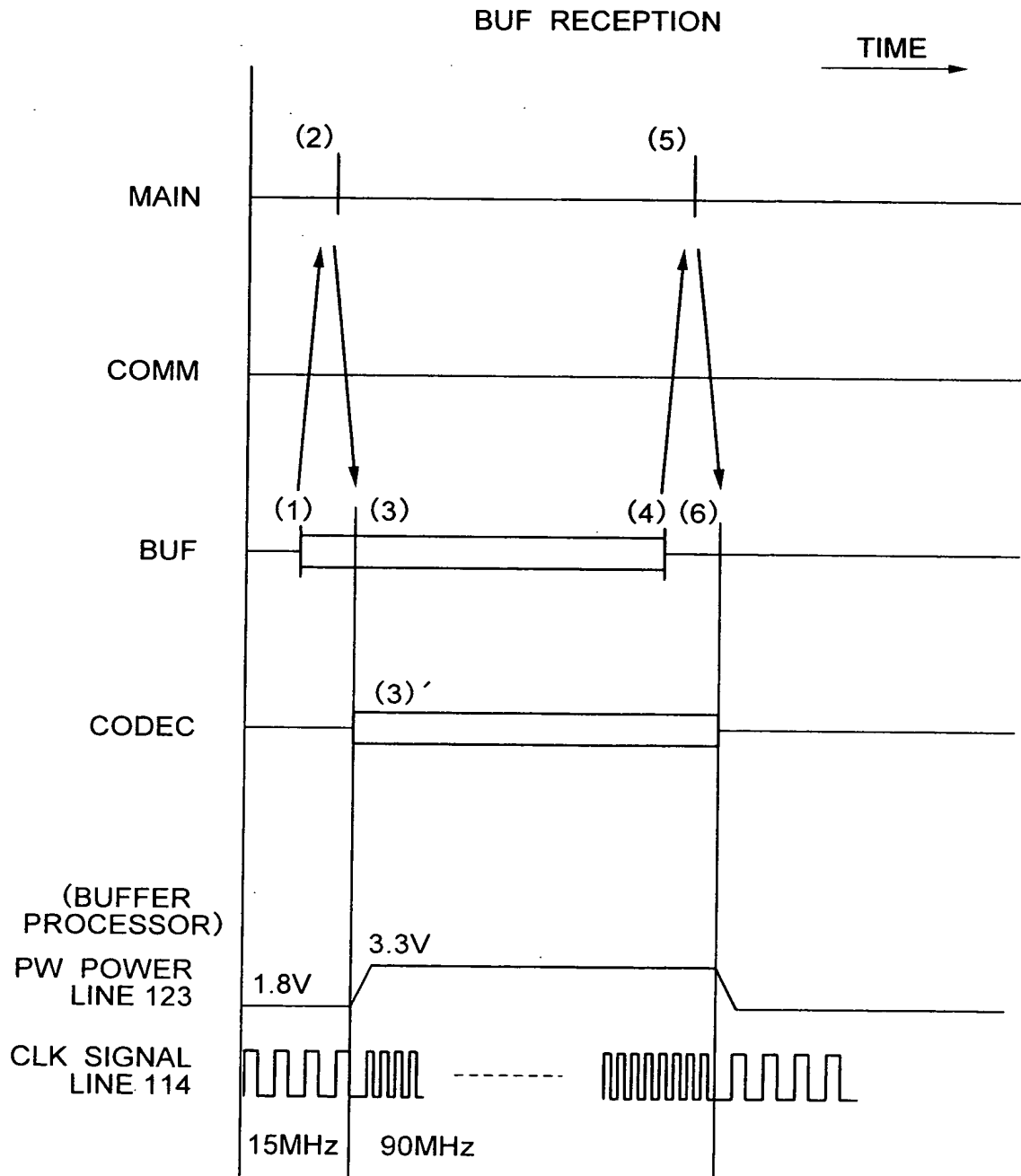


FIG. 9

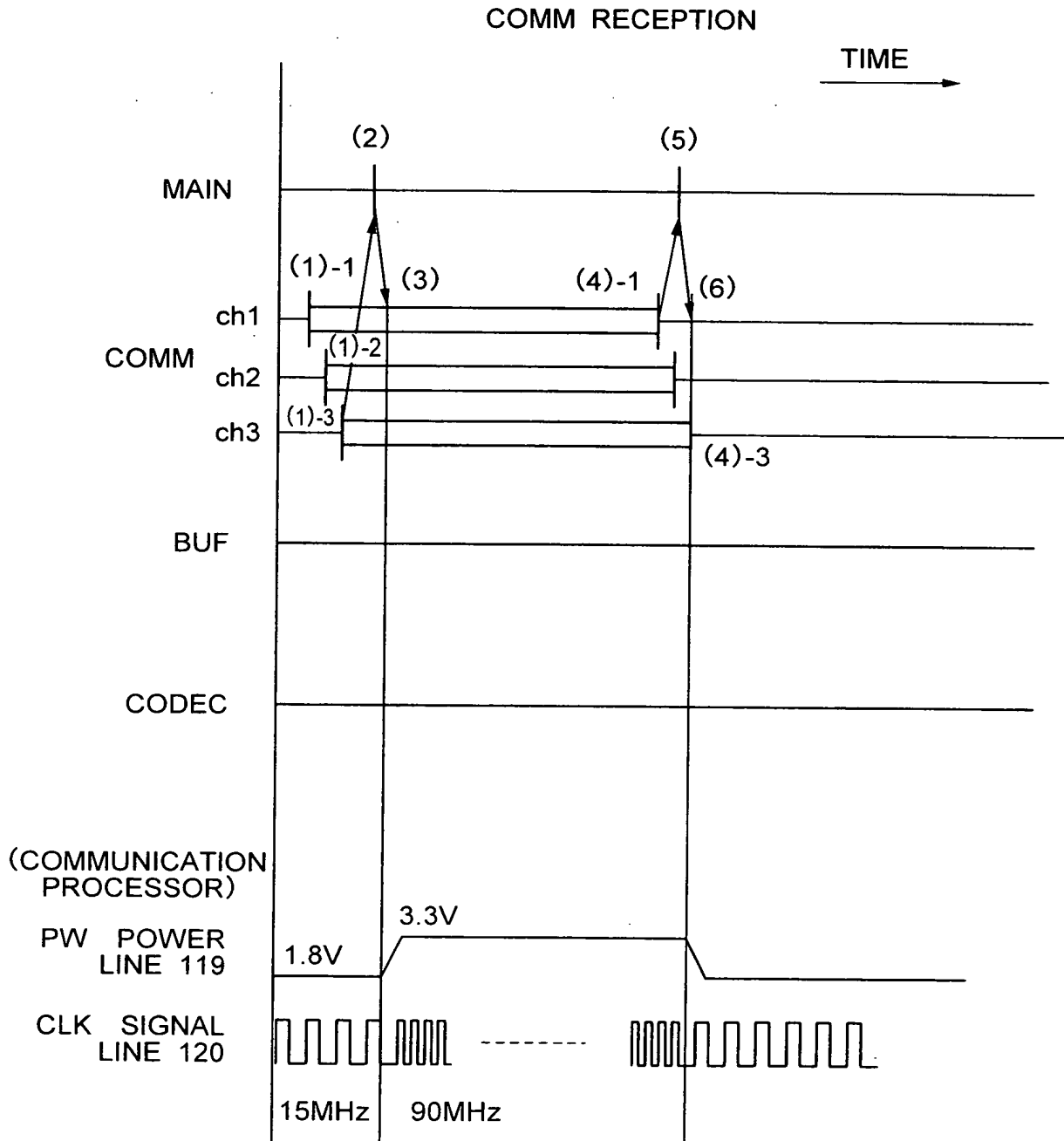


FIG. 10

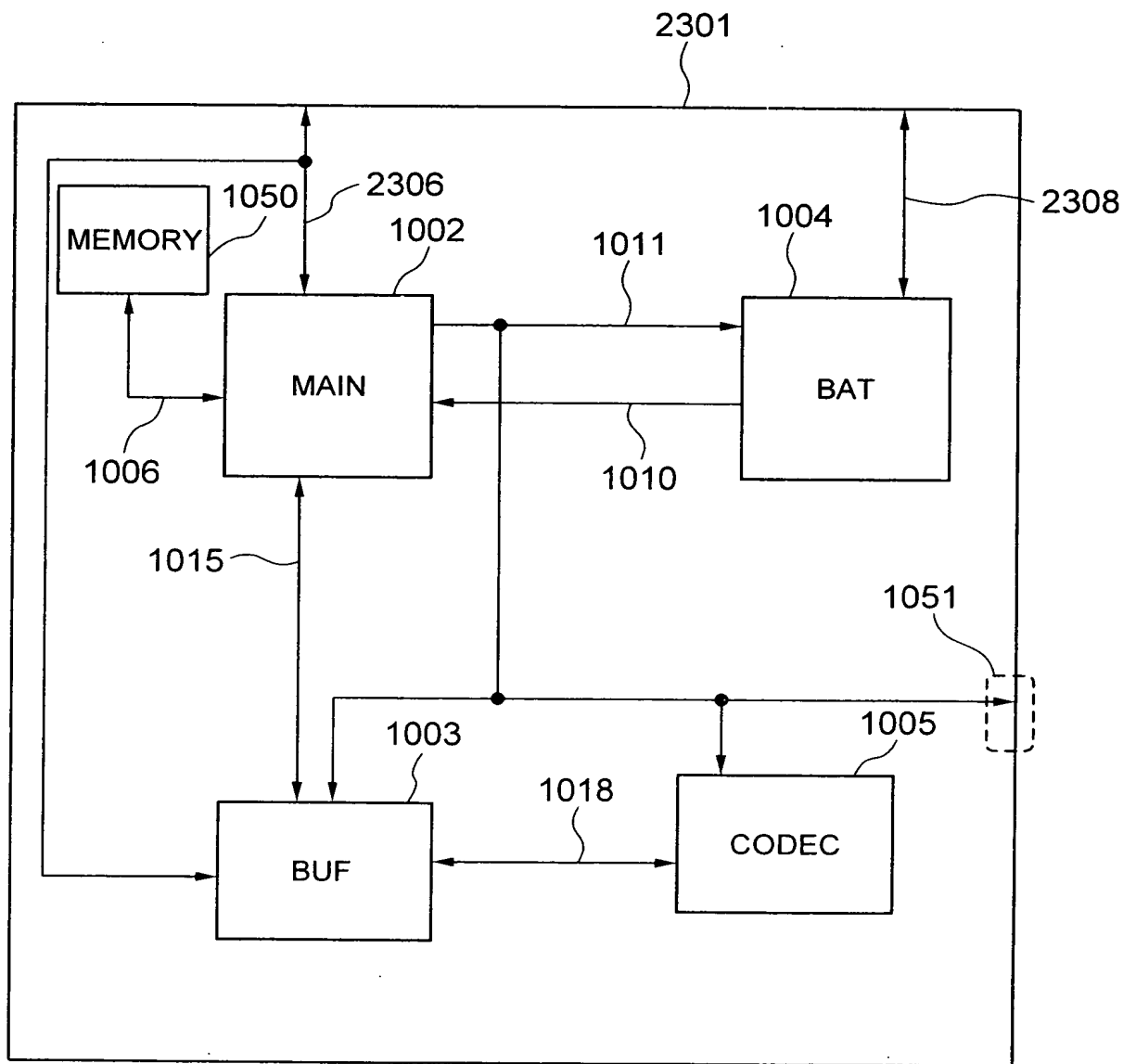


FIG. 11

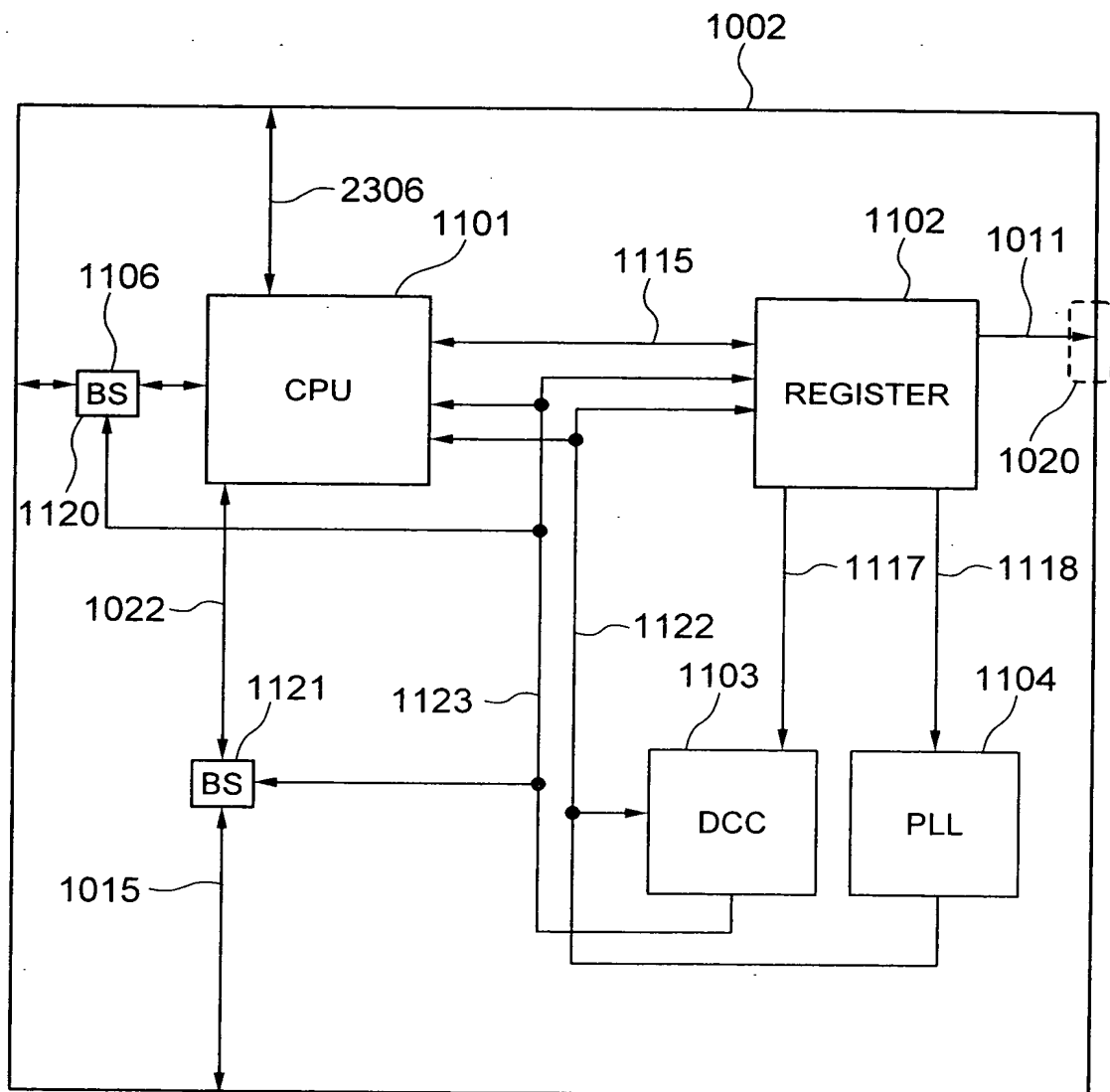


FIG. 12

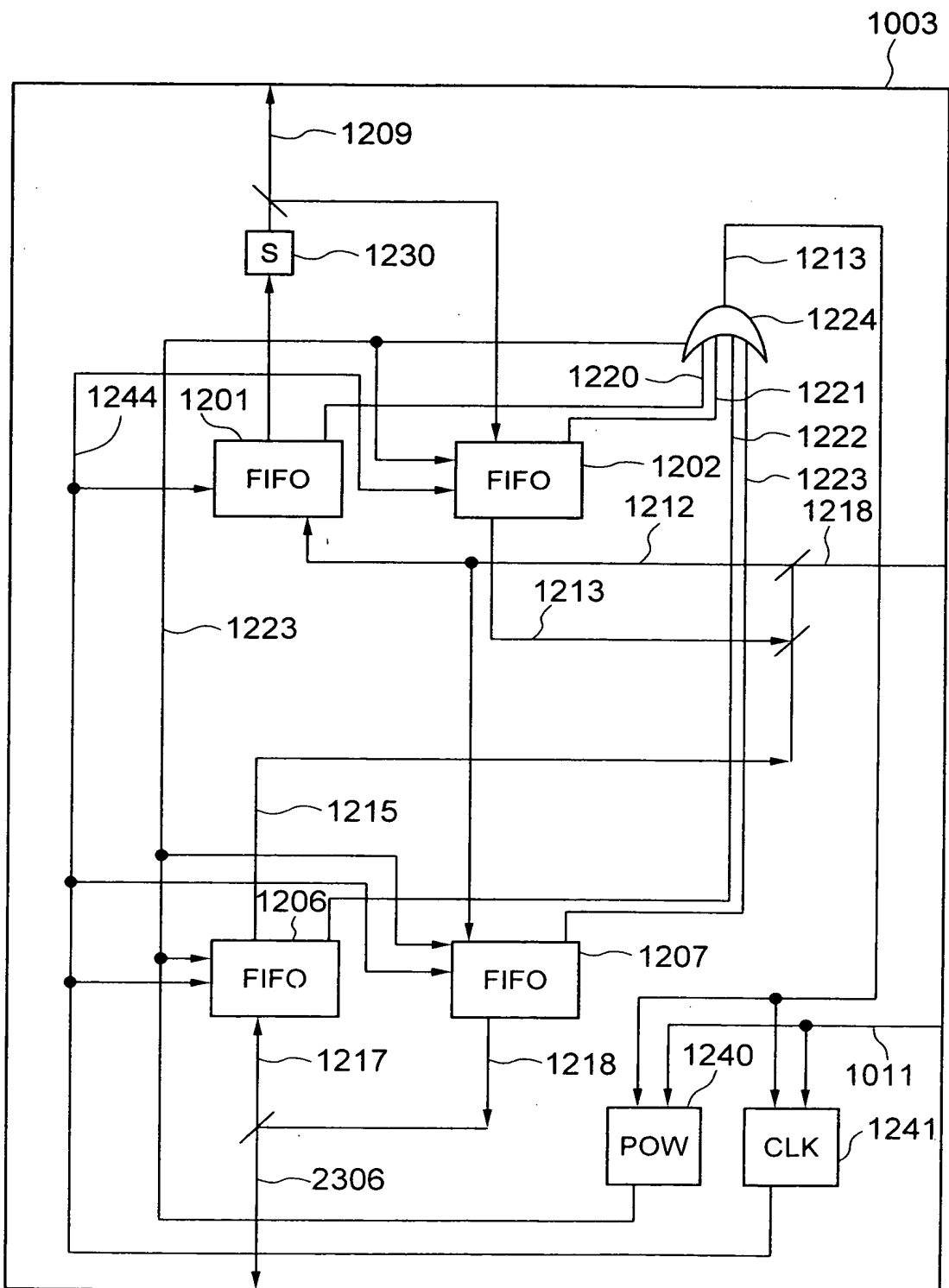


FIG. 13

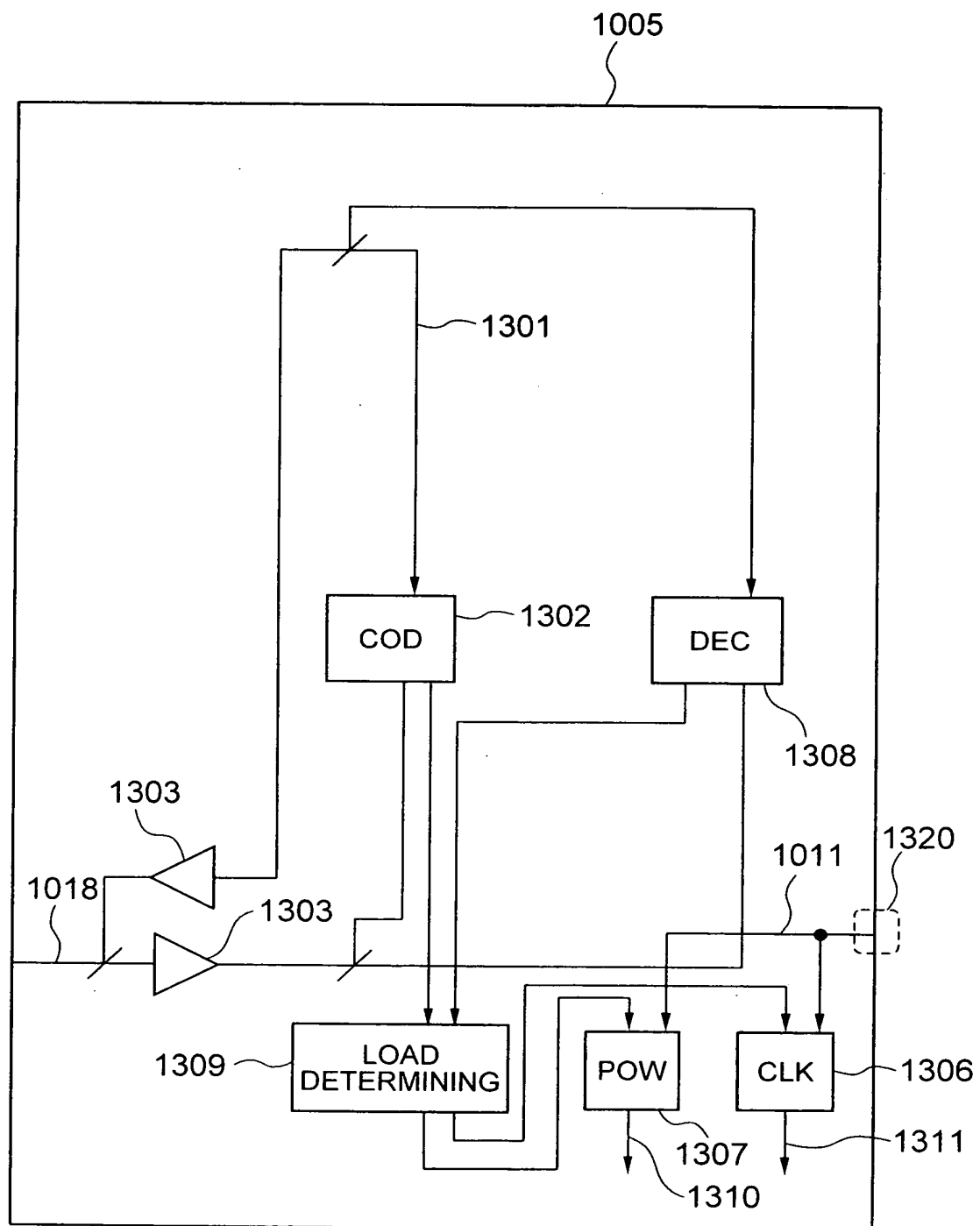


FIG. 14A

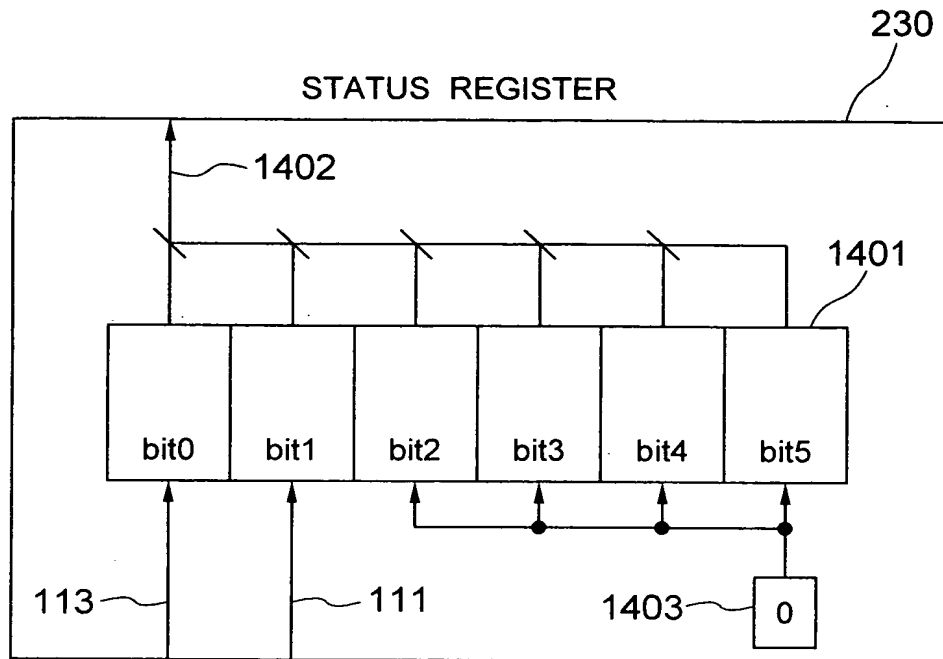


FIG. 14B

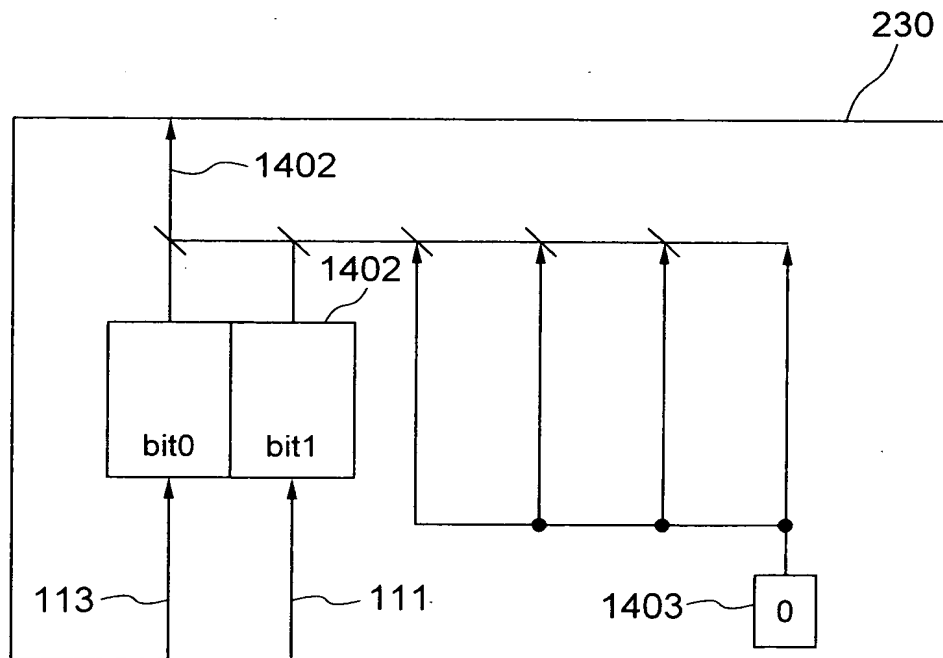


FIG. 15

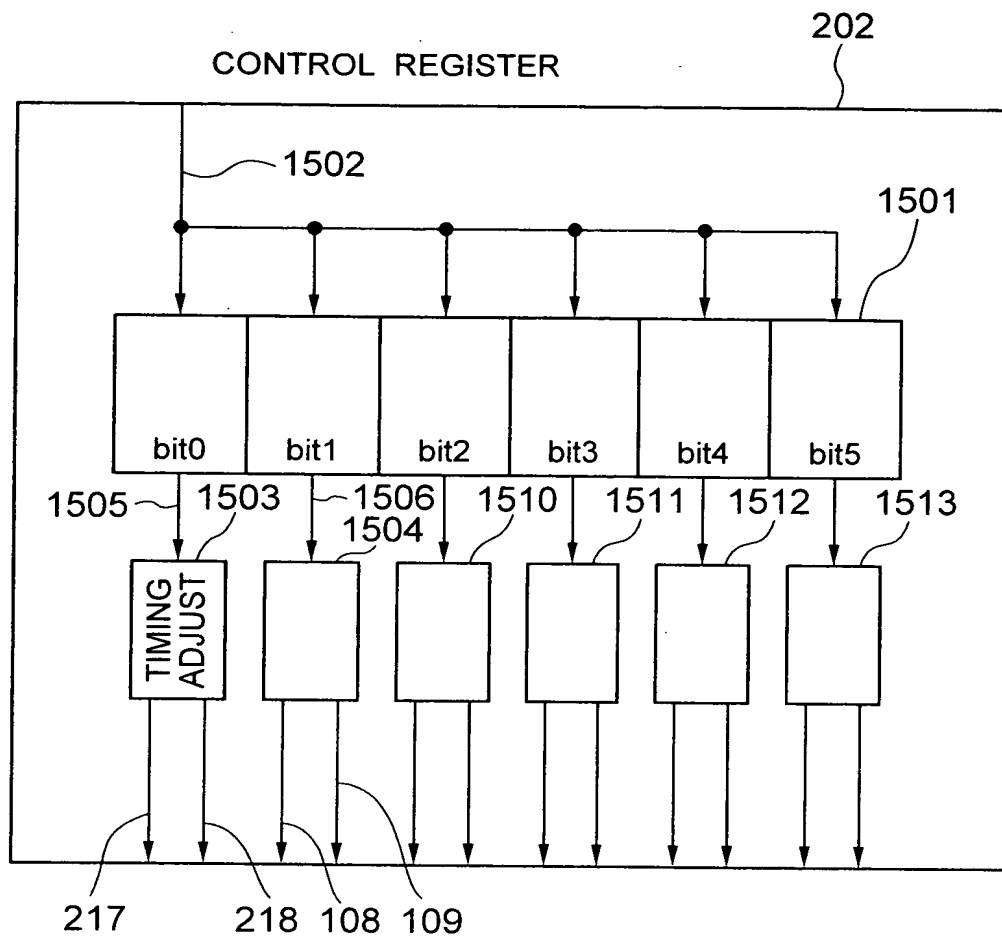


FIG. 16

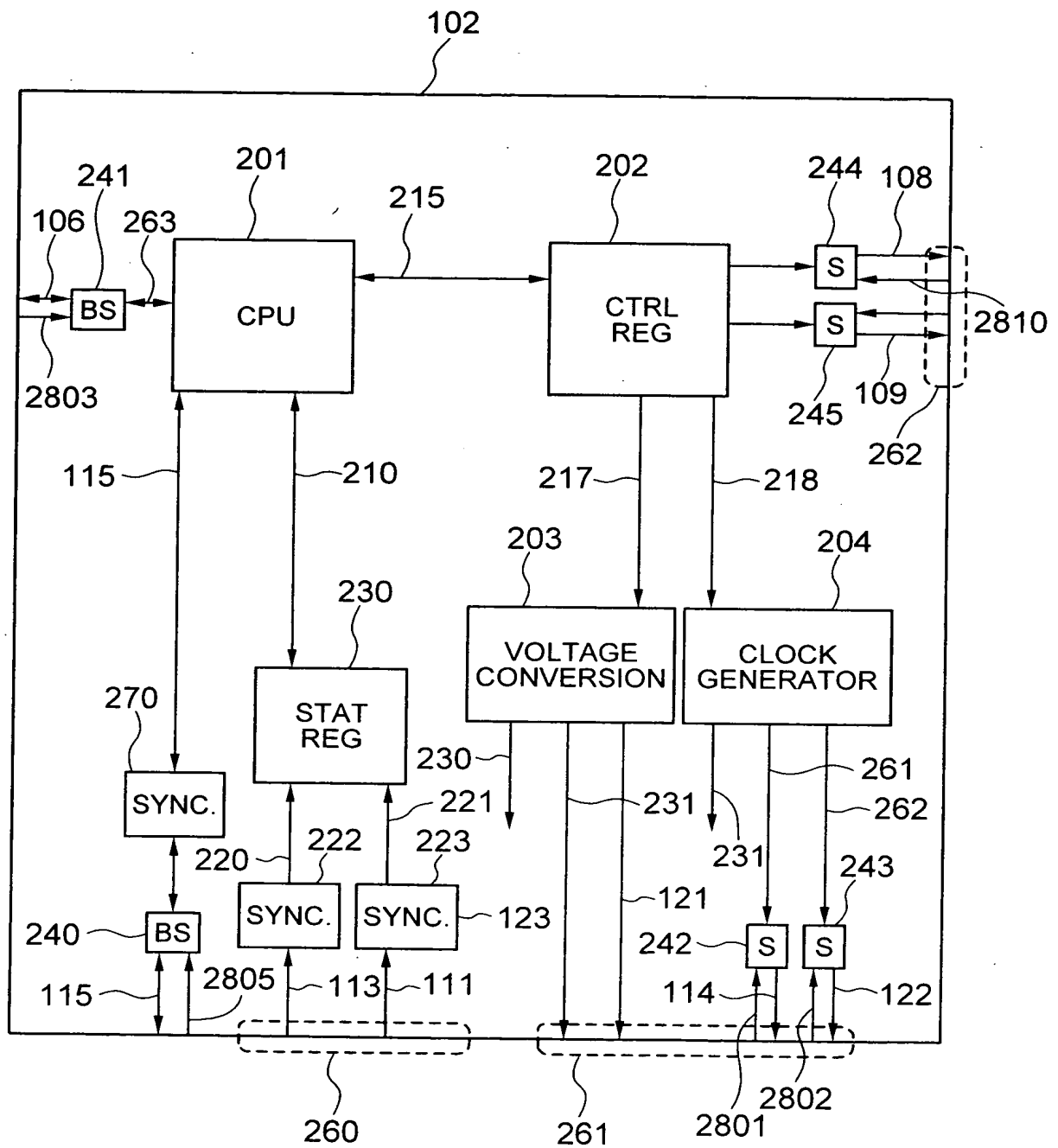


FIG. 17

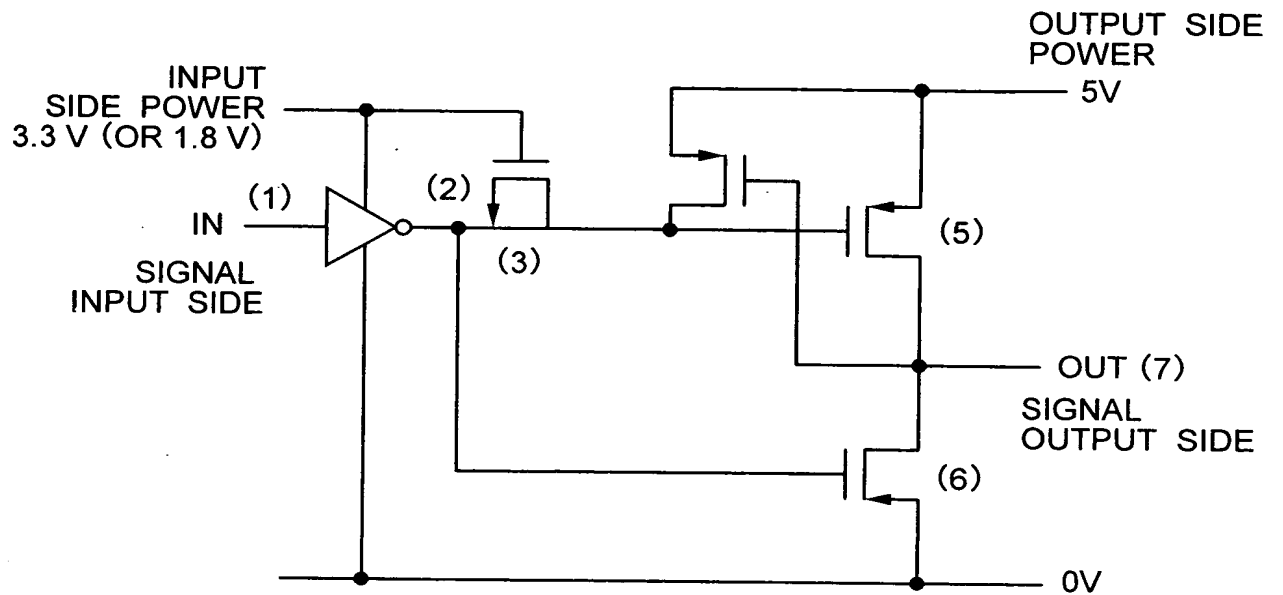


FIG. 18

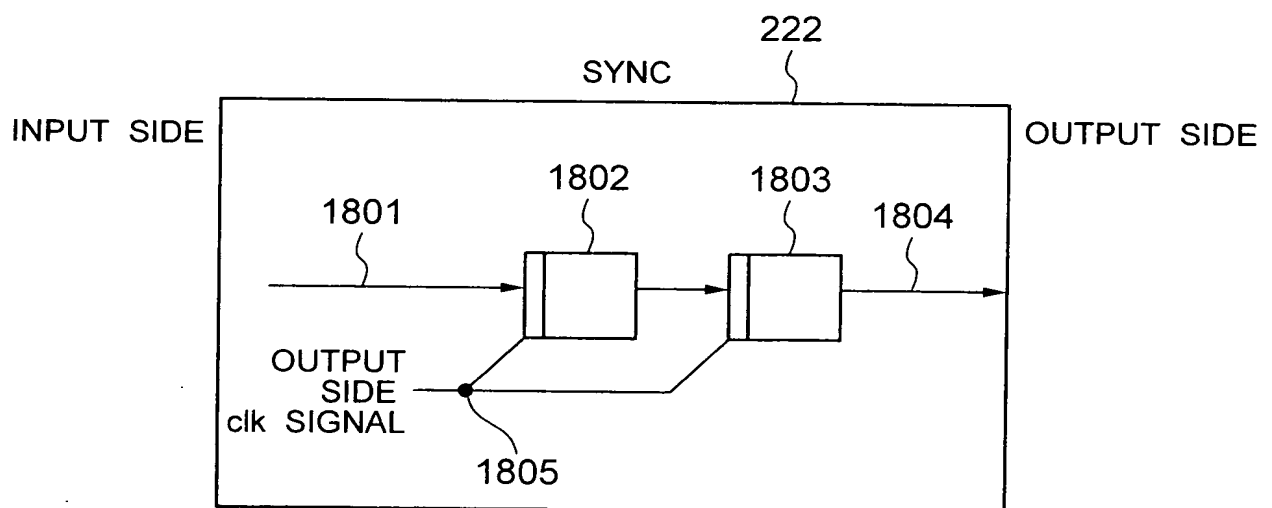


FIG. 19

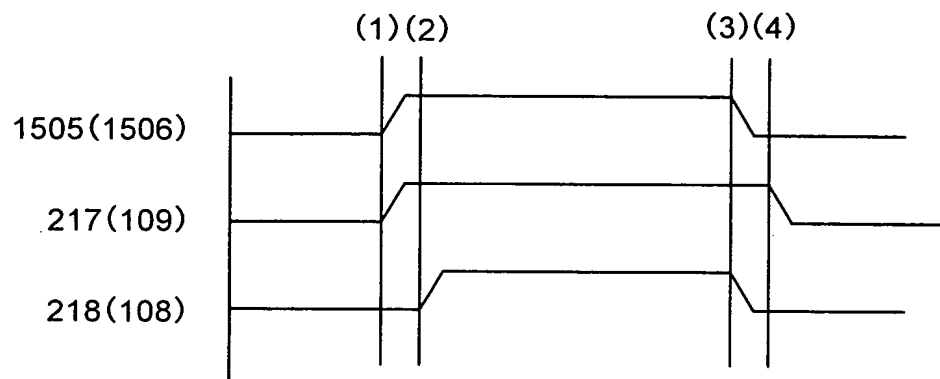


FIG. 20

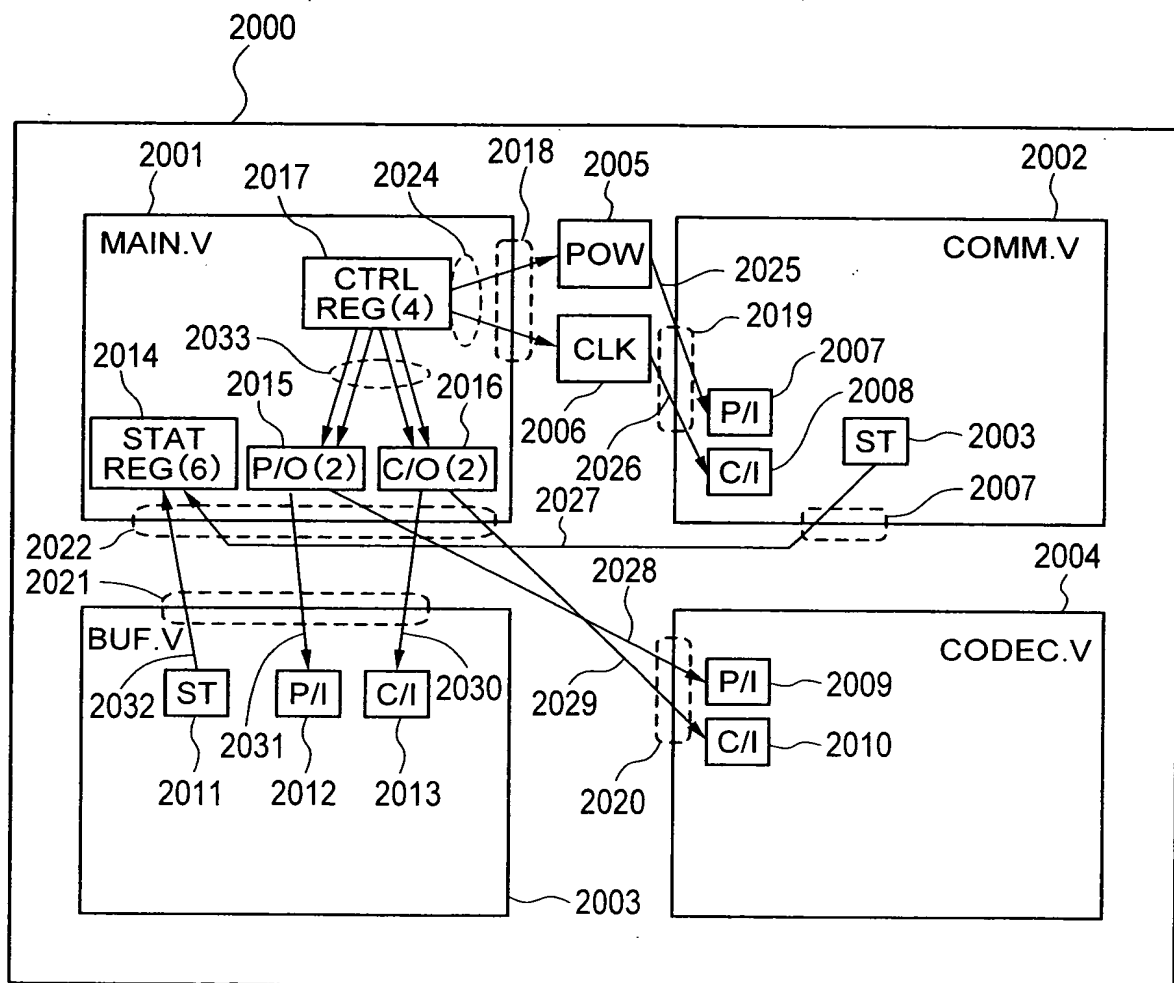


FIG. 21A

```
1: MODULE MAIN(SIG106,...,  
2: //FOR POWER CONTROL INTERFACE  
3:           SIG113,SIG111,  
4:           SIG123,SIG121,  
5:           SIG14,SIG122,  
6:           SIG108,SIG109,  
7: INOUT SIG106,...,  
8: INPUT  SIG113,SIG111,...,  
9: OUTPUT SIG114,SIG122,SIG123,SIG121,...,  
   :  
   :  
   :  
10: ENDMODULE
```

} CIRCUIT DESCRIPTION

FIG. 21B

```
1: MODULE BUF(SIG117,SIG118,  
2: //FOR POWER CONTROL INTERFACE  
3:           SIG144,SIG123,  
4:           SIG113,  
5: INOUT SIG116,SIG117,SIG118;  
6: INPUT SIG123,SIG144;  
7: OUTPUT SIG113;  
   :  
   :  
   :  
8: ENDMODULE
```

} CIRCUIT DESCRIPTION

FIG. 22

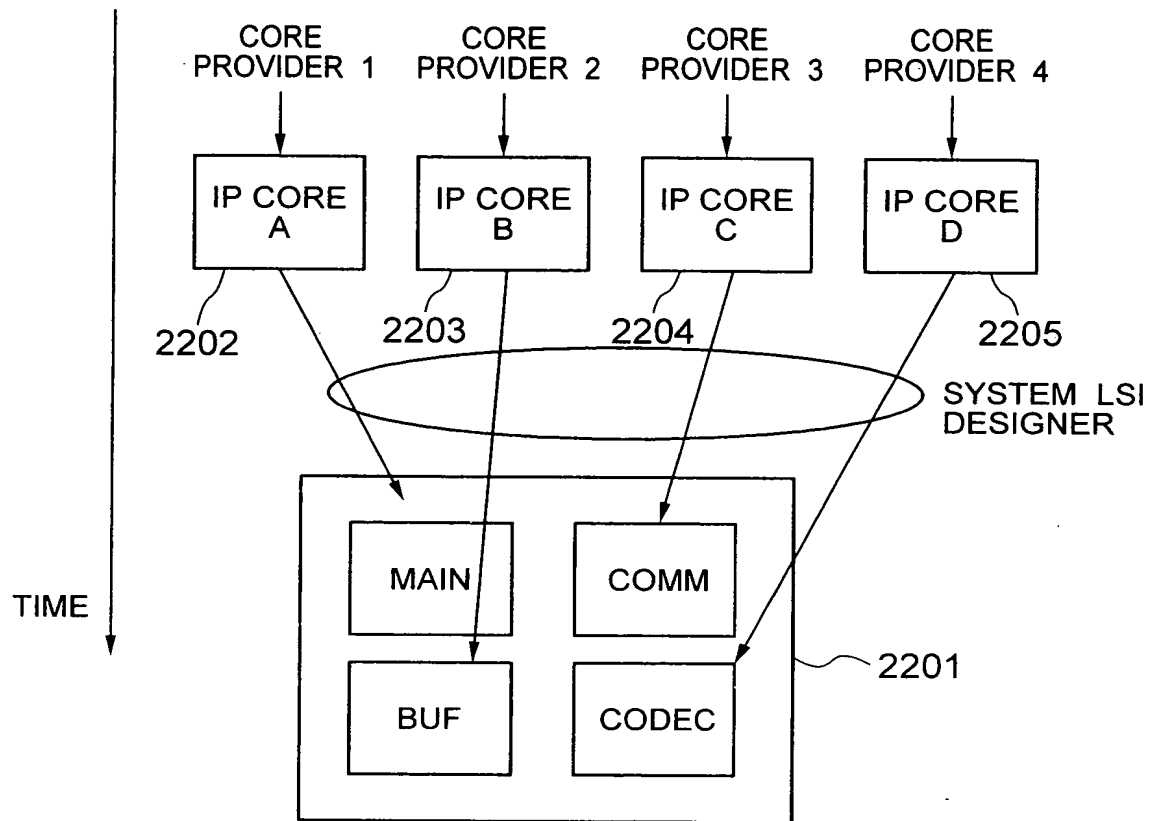


FIG. 23

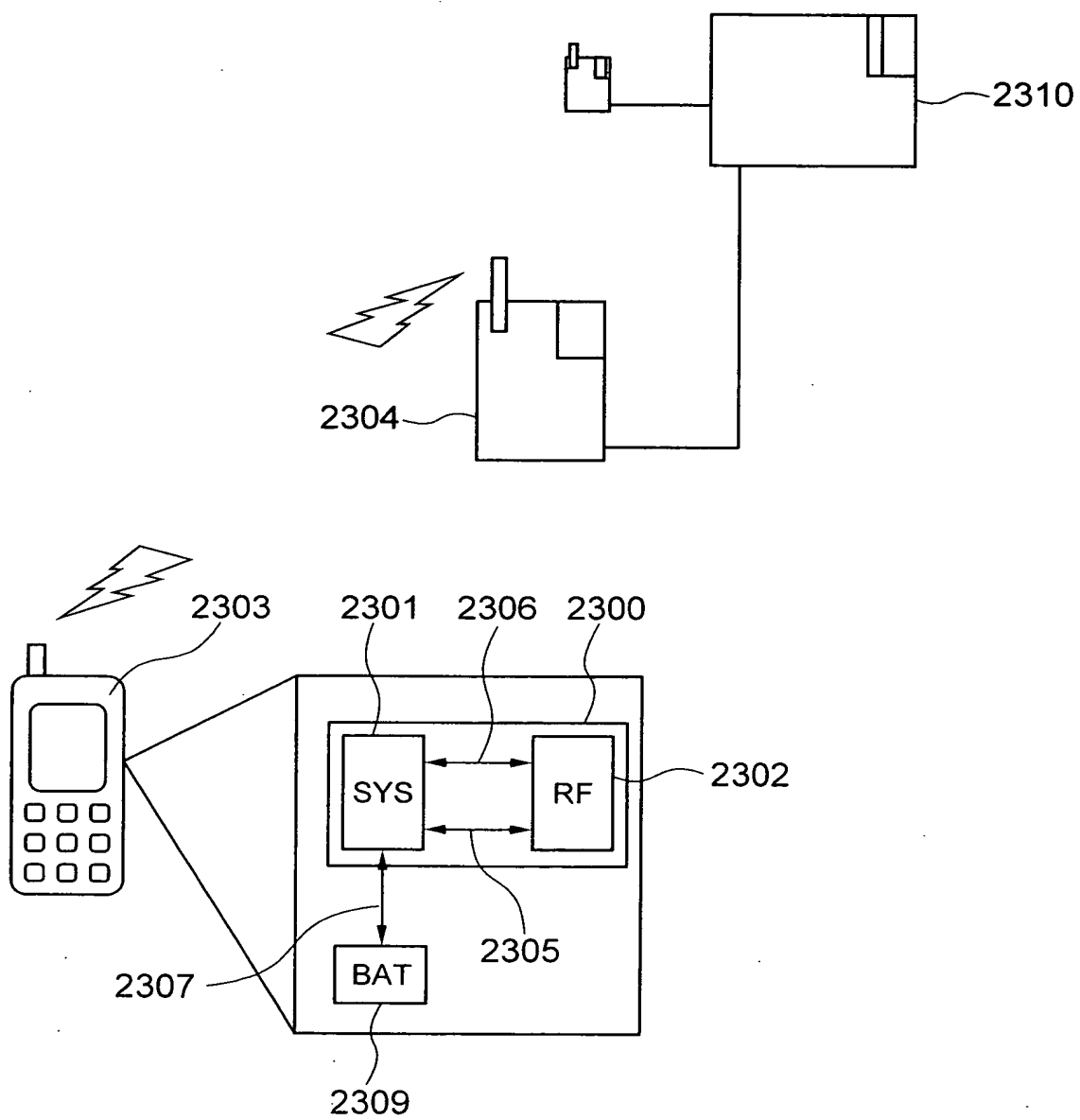


FIG. 24

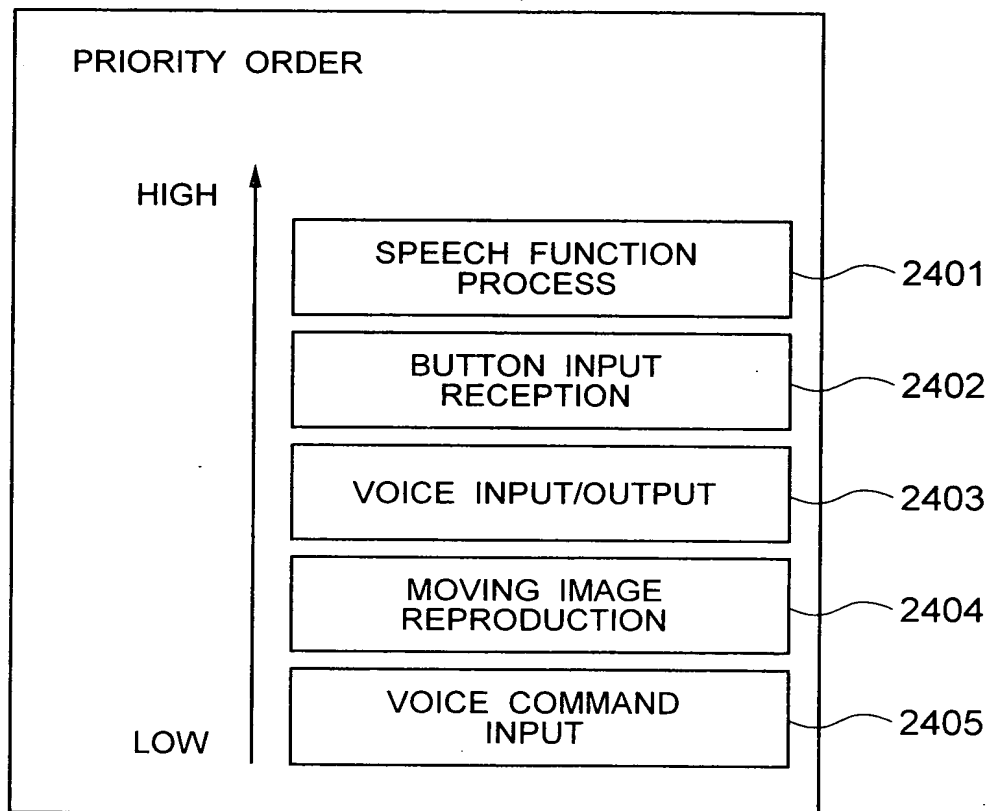


FIG. 25

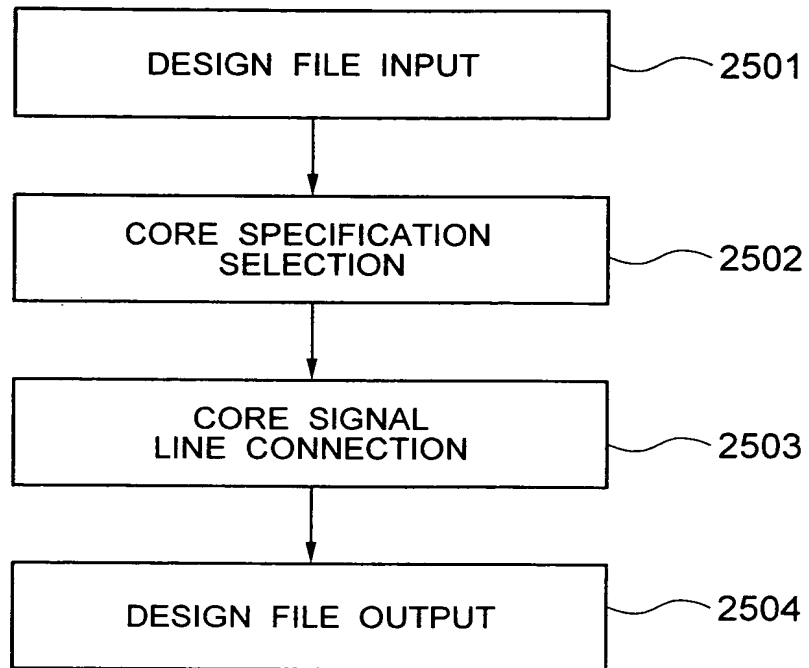


FIG. 26

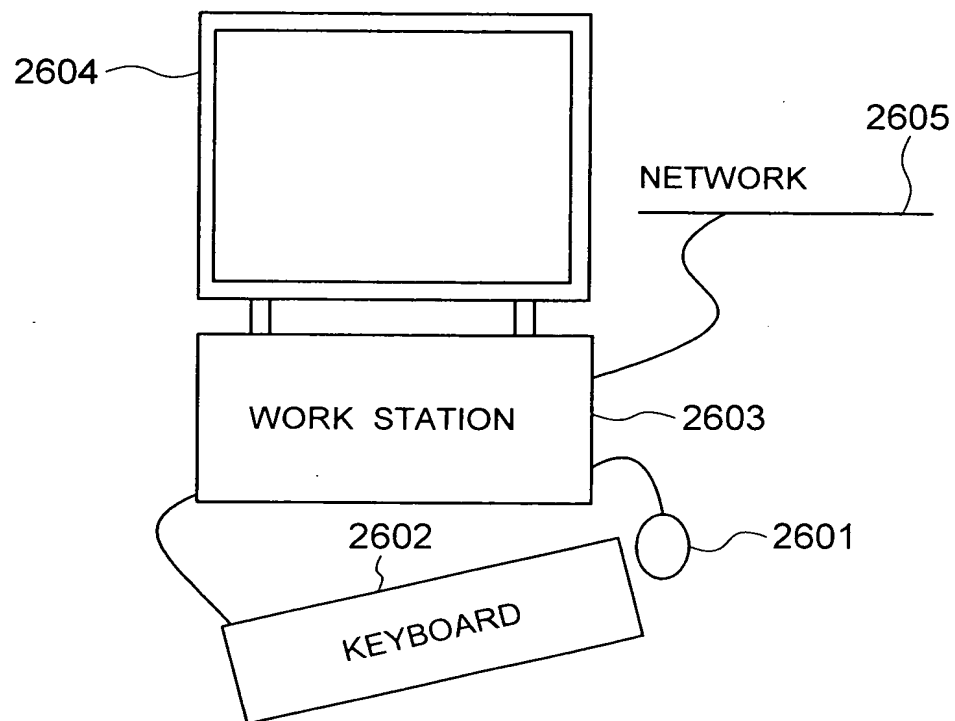


FIG. 27A

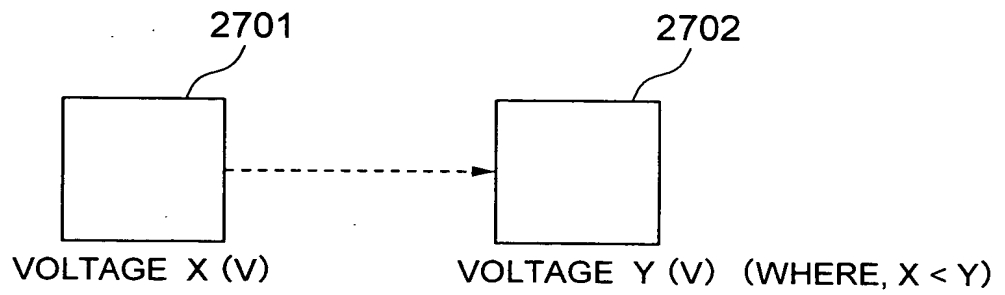


FIG. 27B

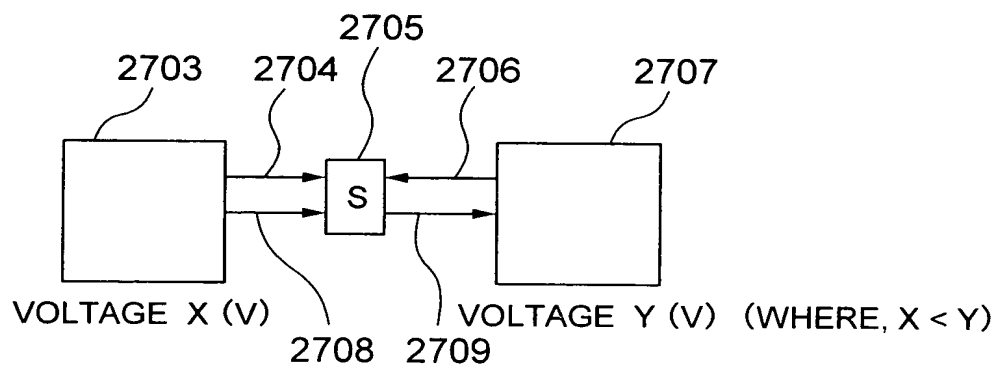


FIG. 27C

